

IN THE CLAIMS

The claims as filed:

- 1 1. (Withdrawn) A method of forming a MOSFET device comprising:
2 providing a substrate;
3 forming on said substrate a relaxed SiGe layer having a Ge content between 0.51
4 and 0.80; and
5 depositing on said relaxed SiGe layer a ϵ -Si layer.
- 1 2. (Withdrawn) The method of claim 1, wherein said ϵ -Si layer is sized approximately at
2 45Å.
- 1 3. (Withdrawn) The method of claim 1 further comprising planarizing said SiGe layer.
- 1 4. (Withdrawn) The method of claim 3, wherein said planarizing comprises CMP.
- 1 5. (Withdrawn) The method of claim 1, wherein said MOSFET device comprises a hole
2 mobility enhancement that increases with effective vertical field.
- 1 6. (Withdrawn) The method of claim 5, wherein said hole mobility enhancement
2 saturates approximately around 2.5.
- 1 7. (Withdrawn) The method of claim 1, wherein said ϵ -Si layer shifts the hole wave
2 function away from the surface of said ϵ -Si layer.
- 1 8. (Withdrawn) The method of claim 1, wherein said substrate comprises a crystalline Si
2 substrate.

1 9. (Withdrawn) The method of claim 1, wherein said substrate comprises a crystalline Si
2 substrate and a relaxed SiGe graded layer.

1 10. (Withdrawn) The method of claim 1, wherein said substrate comprises a crystalline
2 substrate and an insulating layer.

1 11. (Withdrawn) The method of claim 10, wherein said insulator layer comprises an
2 oxide.

1 12. (Withdrawn) The method of claim 1, wherein said MOSFET device comprises a
2 PMOS device.

1 13. (Withdrawn) The method claim 12, wherein said MOSFET device comprises a
2 NMOS device.

1 14. (Withdrawn) The method claim 13, wherein said PMOS and NMOS devices form a
2 CMOS device.

1 15. (Withdrawn) The method of claim 1, wherein said relaxed SiGe layer comprises a
2 selective portion having a Ge content between 0.7 and 0.75.

1 16. (Withdrawn) A method of forming a MOSFET device comprising:
2 providing a substrate;
3 forming on said substrate a relaxed SiGe layer having a Ge content between 0.51
4 and 0.80; and

5 forming on said relaxed SiGe layer a digital alloy structure that comprises
6 alternating layers of ϵ -Si and SiGe having a Ge content between 0.51 and 1, wherein said
7 mobility enhancement of said device is constant.

1 17. (Withdrawn) The method of claim 16, wherein said alternating layers of SiGe and ϵ -
2 Si are sized approximately at 10Å.

1 18. (Withdrawn) The method of claim 16 further comprising planarizing said relaxed
2 SiGe layer.

1 19. (Withdrawn) The method of claim 18, wherein said planarizing comprises CMP.

1 20. (Withdrawn) The method of claim 16, wherein said ϵ -Si layer shifts the hole wave
2 function away from the surface of said ϵ -Si layer.

1 21. (Withdrawn) The method of claim 16, wherein said substrate comprises a crystalline
2 Si substrate.

1 22. (Withdrawn) The method of claim 16, wherein said substrate comprises a crystalline
2 Si substrate and a relaxed SiGe graded layer.

1 23. (Withdrawn) The method of claim 16, wherein said substrate comprises a crystalline
2 substrate and an insulating layer.

1 24. (Withdrawn) The method of claim 23, wherein said insulator layer comprises an
2 oxide.

- 1 25. (Withdrawn) The method of claim 16, wherein said MOSFET device comprises a
2 PMOS device.
- 1 26. (Withdrawn) The method claim 25, wherein said MOSFET device comprises a
2 NMOS device.
- 1 27. (Withdrawn) The method claim 26, wherein said PMOS and NMOS devices form a
2 CMOS device.
- 1 28. (Withdrawn) The method of claim 16, wherein said relaxed SiGe layer comprises a
2 selective portion having a Ge content between 0.7 and 0.75.
- 1 29. (Withdrawn) A method of forming a MOSFET device comprising:
2 providing a substrate;
3 forming on said substrate a relaxed SiGe layer having a Ge content between 0.51
4 and 0.80; and
5 depositing on said relaxed SiGe layer a ϵ -Si layer so that hole mobility
6 enhancement increases with effective vertical field.
- 1 30. (Withdrawn) The method of claim 29, wherein said ϵ -Si layer is sized approximately
2 at 45Å.
- 1 31. (Withdrawn) The method of claim 29 further comprising planarizing said relaxed
2 SiGe layer.
- 1 32. (Withdrawn) The method of claim 31, wherein said planarizing comprises CMP.

- 1 33. (Withdrawn) The method of claim 29, wherein said MOSFET device comprises a
2 hole mobility enhancement that increases with effective vertical field.
- 1 34. (Withdrawn) The method of claim 29, wherein said hole mobility enhancement
2 saturates approximately around 2.5.
- 1 35. (Withdrawn) The method of claim 29, wherein said ϵ -Si layer shifts the hole wave
2 function away from the surface of said ϵ -Si layer.
- 1 36. (Withdrawn) The method of claim 29, wherein said substrate comprises a crystalline
2 Si substrate.
- 1 37. (Withdrawn) The method of claim 29, wherein said substrate comprises a crystalline
2 Si substrate and a relaxed SiGe graded layer.
- 1 38. (Withdrawn) The method of claim 29, wherein said substrate comprises a crystalline
2 substrate and an insulating layer.
- 1 39. (Withdrawn) The method of claim 38, wherein said insulator layer comprises an
2 oxide.
- 1 40. (Withdrawn) The method of claim 29, wherein said MOSFET device comprises a
2 PMOS device.
- 1 41. (Withdrawn) The method of claim 40, wherein said MOSFET device comprises a
2 NMOS device.

1 42. (Withdrawn) The method claim 41, wherein said PMOS and NMOS devices form a
2 CMOS device.

1 43. (Currently Amended) A MOSFET device comprising:
2 a substrate;
3 a relaxed SiGe layer that is formed on said substrate, said relaxed SiGe layer
4 having a Ge content between 0.51 and 0.80 and a selective portion having a Ge content
5 between 0.7 and 0.75; and
6 a ϵ -Si layer that is deposited on said relaxed SiGe layer.

1 44. (Original) The MOSFET device of claim 43, wherein said ϵ -Si layer is sized
2 approximately at 45Å.

1 45. (Original) The MOSFET device of claim 43, wherein said relaxed SiGe layer is
2 planarized.

1 46. (Original) The MOSFET device of claim 43 further comprising a hole mobility
2 enhancement that increases with effective vertical field.

1 47. (Original) The MOSFET device of claim 46, wherein said hole mobility
2 enhancement saturates approximately around 2.5.

1 48. (Original) The MOSFET device of claim 43, wherein said ϵ -Si layer shifts the hole
2 wave function away from the surface of said ϵ -Si layer.

1 49. (Original) The MOSFET device of claim 43, wherein said substrate comprises a
2 crystalline Si substrate.

1 50. (Original) The MOSFET device of claim 43, wherein said substrate comprises a
2 crystalline Si substrate and a relaxed SiGe graded layer.

1 51. (Original) The MOSFET device of claim 43, wherein said substrate comprises a
2 crystalline substrate and an insulating layer.

1 52. (Original) The MOSFET device of claim 51, wherein said insulator layer comprises
2 an oxide.

1 53. (Original) The MOSFET device of claim 43 further comprising a PMOS device.

1 54. (Original) The MOSFET device of claim 53 further comprising a NMOS device.

1 55 (Original). The MOSFET device of claim 54, wherein said PMOS and NMOS
2 devices form a CMOS device.

1 56. (Cancelled)

1 57. (Previously Presented) A MOSFET device comprising:

2 a substrate;

3 a relaxed SiGe layer that is formed on said substrate, said relaxed SiGe layer

4 having a Ge content between 0.51 and 0.80; and

5 a digital alloy structure that is formed on said relaxed SiGe layer comprising

6 alternating layers of ϵ -Si and SiGe having a Ge content between 0.51 and 1, wherein said

7 mobility enhancement of said device is constant.

1 58. (Original) The MOSFET device of claim 57, wherein said alternating layers of SiGe
2 and ϵ -Si is sized approximately at 45Å.

- 1 59. (Original) The MOSFET device of claim 57, wherein said relaxed SiGe layer is
2 planarized.
- 1 60. (Original) The MOSFET device of claim 57, wherein said ϵ -Si layer shifts the hole
2 wave function away from the surface of said ϵ -Si layer.
- 1 61. (Original) The MOSFET device of claim 57, wherein said substrate comprises a
2 crystalline Si substrate.
- 1 62. (Original) The MOSFET device of claim 57, wherein said substrate comprises a
2 crystalline Si substrate and a relaxed SiGe graded layer.
- 1 63. (Original) The MOSFET device of claim 57, wherein said substrate comprises a
2 crystalline substrate and an insulating layer.
- 1 64. (Original) The MOSFET device of claim 63, wherein said insulator layer comprises
2 an oxide.
- 1 65. (Original) The MOSFET device of claim 57 further comprising a PMOS device.
- 1 66. (Original) The MOSFET device claim 65 further comprising a NMOS device.
- 1 67. (Original) The MOSFET device claim 66, wherein said PMOS and NMOS devices
2 form a CMOS device.
- 1 68. (Original) The MOSFET device of claim 57, wherein said relaxed SiGe layer
2 comprises a selective portion having a Ge content between 0.7 and 0.75.
- 1 69. (Currently Amended) A MOSFET device comprising:

2 a substrate;

3 a relaxed SiGe layer that is formed on said substrate, said relaxed SiGe layer

4 having a Ge content between 0.51 and 0.80 and a selective portion having a Ge content

5 between 0.7 and 0.75; and

6 a ϵ -Si layer that is deposited on said relaxed SiGe layer so that hole mobility

7 enhancement increases with effective vertical field.

1 70. (Original) The MOSFET device of claim 69, wherein said ϵ -Si layer is sized

2 approximately at 45Å.

1 71. (Original) The MOSFET device of claim 69, wherein said relaxed SiGe layer is

2 planarized.

1 72. (Canceled)

1 73. (Previously Presented) The MOSFET device of claim 69, wherein said hole mobility

2 enhancement saturates approximately around 2.5.

1 74. (Original) The MOSFET device of claim 69, wherein said ϵ -Si layer shifts the hole

2 wave function away from the surface of said ϵ -Si layer..

1 75. (Original) The MOSFET device of claim 69, wherein said substrate comprises a

2 crystalline Si substrate.

1 76. (Original) The MOSFET device of claim 69, wherein said substrate comprises a

2 crystalline Si substrate and a relaxed SiGe graded layer.

1 77. (Original) The MOSFET device of claim 69, wherein said substrate comprises a
2 crystalline substrate and an insulating layer.

1 78. (Original) The MOSFET device of claim 77, wherein said insulator layer comprises
2 an oxide.

1 79. (Original) The MOSFET device of claim 69 further comprising a PMOS device.

1 80. (Original) The MOSFET device of claim 79 further comprising a NMOS device.

1 81. (Original) The MOSFET device claim 80, wherein said PMOS and NMOS devices
2 form a CMOS device.